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(54) Non-volatile memory device and method of its manufacture.

(57) The present invention discloses a non-volatile memory device having a multi-level gate structure. The storage cell transistor in the cell array region and the transistor in the peripheral circuit region have the same multi-level gate structure. Also, multi-level polycrystalline silicon layers in the peripheral circuit region are connected to each other, and thus utilized as an electrically singular gate electrode. The gate structures of the two regions are formed through a single etching process, so that the decreased processing number of photolithography simplifies overall process, and reduces the damage on the field oxide layer to thereby enhance an insulating performance.

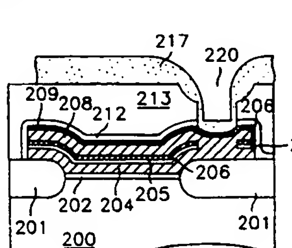

FIG. 3J

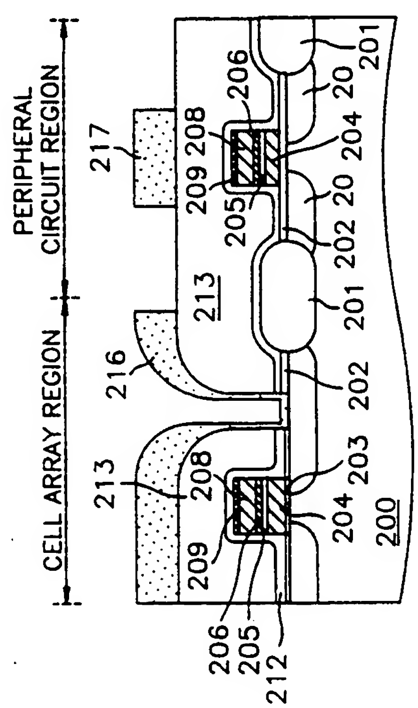

FIG. 3I

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BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor memory device, and more particularly to a non-volatile memory device having a multi-level gate structure.

General non-volatile memory devices of a multi-level gate structure include storage cell transistors having a multi-level gate structure in a cell array region, and transistors having a single-level gate structure for operating the storage cell transistors in a peripheral circuit region. An electrically erasable programmable read only memory (EEPROM) which can be erased and reprogrammed electrically is one type of the memory devices having the multi-level gate structure. A storage cell transistor of the EEPROM has a floating gate electrode for storing data, and a control gate electrode for controlling the floating gate electrode. Also, in the storage cell transistor, an interlayer insulating film is provided between the control gate electrode and floating gate electrode, and a tunnel oxide layer is disposed between the floating gate electrode and a substrate.

A conventional technique for such an EEPROM is disclosed by R. Shirota, et al in IEDM, 1990, pp. 103~106, entitled: "A 2.3mm^2 Memory Cell Structure for 16Mb NAND EEPROMs".

FIGs. 1A to 1J show a process for manufacturing the EEPROM having the multi-level gate structure according to the conventional technique. Here, FIGs. 1A, 1C, 1E, 1G and 1I are longitudinally sectioned views showing a cell array region and peripheral circuit region of the EEPROM manufactured by a sequential process. FIGs. 1B, 1D, 1F, 1H and 1J are sectional views showing the peripheral circuit region laterally cut away from FIGs. 1A, 1C, 1E, 1G and 1I, respectively. Referring to FIGs. 1A and 1B, a field oxide layer 101 is formed on a substrate 100 by a common LOCal Oxidation of Silicon (LOCOS). Then, a gate oxide layer 105 is formed on the whole surface of the substrate 100, and the gate oxide layer 105 to have a storage cell transistor in the cell array region thereon is etched by a photolithography. Thereafter, a thin tunnel oxide layer 102 is formed on the surface of the substrate 100 in the portion of forming the storage cell transistor. A first polycrystalline silicon layer 103 and an ONO (oxide/nitride/oxide) layer 104 which is an interlayer insulating film are sequentially formed on the whole surface of the substrate 100. Thereafter, using a photoresist pattern 106 as a mask, these layers just on the peripheral circuit region are sequentially etched by a common etching method, to thus expose the surfaces of the field oxide layer 101 and substrate 100. The first polycrystalline silicon layer 103 is a conductive layer for a floating gate electrode of the storage cell transistor. Referring to FIGs. 1C and 1D, after removing the photoresist pattern 106, a gate oxide layer 107 is formed on the substrate 100 in the peripheral circuit region through a thermal oxidation, and a second polycrystalline silicon layer 108 and a tungsten silicide layer 109 are sequentially formed on the whole surface of the substrate 100. The second polycrystalline silicon layer 108 and tungsten silicide layer 109 form a control gate electrode of the storage cell transistor and a gate electrode of the transistor in the peripheral circuit region. Referring to FIGs. 1E and 1F, a photoresist pattern 110 is formed on the peripheral circuit region to form the gate electrode of the transistor. The tungsten silicide layer 109 and second polycrystalline silicon layer 108 are etched to expose the surface of the field oxide layer 101 and the gate oxide layer 107. Thereafter, an ion-implantation is performed to form source and drain regions of the transistor in the peripheral circuit region. Referring to FIGs. 1G and 1H, after removing the photoresist pattern 110, a photoresist pattern 111 is formed on the cell array region. The tungsten silicide layer 109, the second polycrystalline silicon layer 108, the ONO layer 104 and the first polycrystalline silicon layer 103 are then etched sequentially until the surface of the tunnel oxide layer 102 and the gate oxide layer 105 is exposed, thereby forming a storage cell transistor. Next, an ion-implantation is performed to form source and drain regions of the storage cell transistor. Referring to FIGs. 1I and 1J, after removing the photoresist pattern 111, a drive-in is performed to form the source and drain regions of the transistor in the peripheral circuit region, and the source and drain regions of the storage cell transistor in the cell array region. An insulating layer of a low-temperature oxide (LTO) layer 112 and a borophosphorous silicate glass (BPSG) layer 113 are sequentially formed on the whole surface of the substrate 100, and a reflow process is performed. Finally, an opening is formed in the portions of the cell array region and the peripheral circuit region which will be contacted with metal layers 114 and 115 respectively, and then, the metal layers 114 and 115 are formed.

In the memory device having the multi-level gate structure manufactured by the conventional technique shown in FIGs. 1A to 1J, since the gate structure of the storage cell transistor 12 in the cell array region differs from that of the transistor 11 in the peripheral circuit region, another photolithography processes are required as shown in FIGs. 1A, 1E and 1G. Due to this fact, the ONO layer which is the interlayer insulating film is contaminated owing to an organic photoresist. Moreover, the damage on the field oxide layer resulting from increased etching processes degrades an insulat-

ing performance, and complicates the manufacturing process.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a non-volatile memory device, wherein a storage cell transistor and a transistor in a peripheral circuit region have the same multi-level gate structure.

It is another object of the present invention to provide a method for manufacturing a non-volatile memory device having a multi-level gate structure formed by a single photolithography process while gate electrodes of a storage cell transistor and a transistor in a peripheral circuit region have the same multi-level structure.

It is still another object of the present invention to provide a method for manufacturing a non-volatile memory device having a multi-level gate structure, wherein an interlayer insulating film is prevented from being contaminated, thereby providing an excellent interlayer insulating performance.

According to one feature of the present invention, the gate electrode of the transistor in the peripheral circuit region has a multi-level structure which is the same as the gate electrode of the storage cell transistor in the cell array region, and the multi-level gate electrodes of the transistor in the peripheral circuit region are connected to each other, thereby functioning as a single gate electrode.

According to another feature of the present invention, the gate electrode of the transistor in the peripheral circuit region has a multi-level structure which is the same as the gate electrode of the storage cell transistor in the cell array region, and the multi-level gate electrodes of the transistor in the peripheral circuit region are connected to each other, so that the storage cell transistor and transistor in the peripheral circuit region can be formed by a single photolithography process.

According to still another feature of the present invention, a polycrystalline silicon layer for preventing contamination is provided on the interlayer insulating film.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and other advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIGs. 1A to 1J show a process for manufacturing a non-volatile memory device by a conventional technique;

FIG. 2 shows a layout of the peripheral circuit region of a non-volatile memory device according to the present invention; and

FIGs. 3A to 3J show one embodiment of a process for manufacturing a non-volatile memory device according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 2 is a layout of the peripheral circuit region of a non-volatile memory device according to the present invention, wherein a line A-A' is a section line for illustrating source and drain regions 20 of a peripheral circuit region, and a line B-B' is a section line for illustrating the shapes of a contact hole between first and third polycrystalline silicon layers and a contact hole between the third polycrystalline silicon layer and a metal layer. A reference numeral 201 designates a field oxide layer; 20 is an active region having source and drain regions thereon; 210 is a contact hole pattern between the first and third polycrystalline silicon layers; 220 is a contact hole pattern between the third polycrystalline silicon layer and the metal layer; 209 is a silicide layer pattern which is an upper layer of a multi-level conduction layer stacked sequentially; and 217 is a metal layer pattern in contact with the third polycrystalline silicon layer via the contact hole 220.

FIGs. 3A to 3J show a process for manufacturing one embodiment of an EEPROM according to the present invention. FIGs. 3A, 3C, 3E, 3G and 3I are longitudinally sectioned views showing a cell array region and peripheral circuit region of the EEPROM manufactured by a sequential process, taken along the line A-A' of FIG. 2. FIGs. 3B, 3D, 3F, 3H and 3J are sectional views showing the peripheral circuit region laterally cut away from FIGs. 3A, 3C, 3E, 3G and 3I respectively, taken along the line B-B' of FIG. 2. Referring to FIGs. 3A and 3B, a field oxide layer 201 is formed on a semiconductor substrate 200 by a common LOCOS, and a gate oxide layer 202 is formed on the whole surface of the substrate 200. Then, the gate oxide layer 202 to have a storage cell transistor in the cell array region thereon is etched by a photolithography, and a thin tunnel oxide layer 203 is formed on the surface of the substrate 200 in the portion of forming the storage cell transistor. Generally, the tunnel oxide layer 203 is so thin by a thickness of below 200Å. In FIGs. 3C and 3D, a first polycrystalline silicon layer 204 of a floating gate electrode, an ONO layer 205 of an interlayer insulating film, and a second polycrystalline silicon layer 206 are sequentially formed on the whole surface of the substrate 200. The second polycrystalline silicon layer 206 and the interlayer insulating film 205 in the peripheral circuit region are partially etched by a photolithography to expose a

portion of the surface of the first polycrystalline silicon layer 204, thereby forming a contact hole 210. Preferably, the second polycrystalline silicon layer 206 is thin to have a thickness of about 200 to 500Å, and functions for preventing the interlayer insulating film 205 from being contaminated by a photoresist pattern 207 composed of an organic material. In this embodiment, the ONO layer is utilized as the interlayer insulating film, but an oxide layer or another insulating layer may be alternatively used. Referring to FIGs. 3E and 3F, the photoresist pattern 207 is removed, and a third polycrystalline silicon layer 208 for a control gate electrode and a silicide layer 209 are sequentially formed on the whole surface of the substrate 200. Referring to FIGs. 3G and 3H, photoresist patterns 211a and 211b are formed in the cell array region and the peripheral circuit region, and the silicide layer 209, third polycrystalline silicon layer 208, second polycrystalline silicon layer 206, interlayer insulating film 205 and first polycrystalline silicon layer 204 are sequentially etched by a photolithography to form the gate electrodes of the storage cell transistor and the transistor in the peripheral circuit region. After this, an ion-implantation is performed to form source and drain regions. During performing the steps illustrated with reference to FIG. 3E, a wet-etch process may be added for eliminating a natural oxide existing on the surface of the second polycrystalline silicon layer 206 which has been formed prior to depositing the third polycrystalline silicon layer 208. As shown in FIG. 3F, it can be noted that the first polycrystalline silicon layer 204 and the third polycrystalline silicon layer 208 are in contact with each other via the contact hole 210 of the peripheral circuit region. Accordingly, the first and third polycrystalline silicon layers serve as a single gate electrode in the peripheral circuit region. In FIGs. 3G and 3H, since the gate electrodes of the storage cell transistor and transistor in the peripheral circuit region are completed through the photolithography process once, the number of processing is decreased as compared with that of the conventional technique. As shown in FIGs. 3I and 3J, after removing the photoresist patterns 211a and 211b, a drive-in process is executed to form source and drain regions of the transistor in the peripheral circuit region and those of the storage cell transistor in the cell array region. A LTO insulating layer 212 and a BPSG layer 213 are sequentially formed on the whole surface of the substrate 200 and a reflow process is performed. Finally, metal layers 216 and 217 are formed after forming contact holes in the cell array region and the peripheral circuit region. The metal layer 217 in the peripheral circuit region is preferably connected in a contact hole 220. As shown in FIG. 3J, since the lower floating gate electrode (the first polycrystalline silicon layer 204) and the upper control gate electrode (the third polycrystalline silicon layer 208) are connected to each other, the gate electrodes of the transistor in the peripheral circuit region operate as a single gate electrode. At this time, the lower floating gate electrode actually functions as the gate electrode of the transistor.

In the memory device having the multi-level gate structure according to the present invention as described above, the storage cell transistor in the cell array region and the transistor in the peripheral circuit region have the same multi-level gate structure. Also, multi-level polycrystalline silicon layers in the peripheral circuit region are connected to each other, and thus utilized as an electrically singular gate electrode. The gate structures of the two regions are formed through a single etching process, so that the decreased processing number of photolithography simplifies overall process, and reduces the damage on the field oxide layer to thereby enhance an insulating performance. Furthermore, since the photolithography process is carried out after thinly depositing the polycrystalline silicon on the surface of the interlayer insulating film, the interlayer insulating film is prevented from being contaminated owing to the photolithography process, thereby providing a non-volatile memory device having an excellent insulating effect of the interlayer insulating film.

While the present invention has been particularly shown and described with reference to particular embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be effected therein without departing from the spirit and scope of the invention as defined by the appended claims.

Claims

1. In a semiconductor memory device having a storage cell transistor being formed in a cell array region comprising a field oxide layer formed on a substrate, a tunnel oxide layer formed on the surface of said substrate, a floating gate electrode formed on the surface of said tunnel oxide layer, an interlayer insulating film formed on the surface of said floating gate electrode, and a control gate electrode formed on the surface of said interlayer insulating film, said semiconductor memory device comprising:

   a transistor being formed in a peripheral circuit region comprising a gate oxide layer formed on the surface of said substrat , said floating gate electrode formed on the surface of said gate oxide layer, said interlayer insulating film formed on the surface of said floating gate electrode, and said control gate electrode

formed on the surface of said interlayer insulating film and connected to said floating gate electrode in a predetermined portion, whereby said control gate electrode and said floating gate electrode serve as a single gate electrode.

2. A semiconductor memory device as claimed in claim 1, wherein said floating gate electrode and control gate electrode are formed of a polycrystalline silicon.

3. A semiconductor memory device as claimed in claim 1, wherein said interlayer insulating film is a multi-level insulating layer having a structure of oxide/nitride/oxide layer.

4. A semiconductor memory device as claimed in claim 1, further comprising a thin polycrystalline silicon layer for preventing contamination of said interlayer insulating film formed between said interlayer insulating film and control gate electrode.

5. A semiconductor memory device as claimed in claim 1, wherein said control gate electrode is a double layer obtained by stacking a polycrystalline silicon layer and a silicide layer.

6. A semiconductor memory device as claimed in claim 5, wherein said silicide layer is formed of tungsten silicide.

7. A non-volatile memory device comprising:

a plurality of storage cell transistors comprising source and drain regions of a second conductivity type formed on a substrate of a first conductivity type and separated from each other by a predetermined distance, a tunnel oxide layer formed on the surface of said substrate between said source and drain regions, a floating gate electrode formed on the surface of said tunnel oxide layer, an interlayer insulating film formed on the surface of said floating gate electrode, and a control gate electrode formed on the surface of said interlayer insulating film;

a plurality of peripheral transistors comprising a gate oxide layer at least thicker than said tunnel oxide layer, and a gate electrode formed on the surface of said gate oxide layer, wherein said gate electrode has said floating gate electrode and said control gate electrode electrically connected to each other.

8. A non-volatile memory device as claimed in claim 7, wherein said floating gate electrode and control gate electrode are formed of a polycrystalline silicon.

9. A non-volatile memory device as claimed in claim 7, wherein said interlayer insulating film is a multi-level insulating layer having a structure of oxide/nitride/oxide layer.

10. A non-volatile memory device as claimed in claim 7, further comprising a thin polycrystalline silicon layer for preventing contamination of said interlayer insulating film formed between said interlayer insulating film and control gate electrode.

11. A non-volatile memory device as claimed in claim 7, wherein said control gate electrode is a double layer obtained by stacking a polycrystalline silicon layer and a silicide layer.

12. A method for manufacturing a semiconductor memory device comprising:

a first step of forming a field oxide layer on a substrate for separating said substrate into a cell array region and a peripheral circuit region, forming a gate oxide layer on the whole surface of said substrate other than said field oxide layer, removing said gate oxide layer on a portion to have a gate electrode of a storage cell transistor in said cell array region thereon, and forming a tunnel oxide layer on said portion to have said storage cell transistor thereon;

a second step of sequentially forming a first polycrystalline silicon layer of a floating gate electrode, an interlayer insulating film, and a second polycrystalline silicon layer for preventing contamination of said interlayer insulating film, and exposing a portion of the surface of said first polycrystalline silicon layer by partially etching said second polycrystalline silicon layer and interlayer insulating film formed on said peripheral circuit region to form a contact hole;

a third step of sequentially forming a third polycrystalline silicon layer and silicide layer of a control gate electrode on the whole surface of said substrate, patterning in said cell array region and said peripheral circuit region to sequentially etch said silicide layer, said third polycrystalline silicon layer, said second polycrystalline silicon layer, said interlayer insulating film, and said first polycrystalline silicon layer by a photolithography process, and implanting an ion for forming source and drain regions; and

a fourth step of forming said source and drain regions by a driv -in process, forming a low-temperature oxide layer and a

borophosphorous silicate glass layer on the whole surface of said substrate prior to performing a reflow process, and forming metal layers in said cell array region and peripheral circuit region.

13. A method for manufacturing a semiconductor memory device as claimed in claim 12, wherein said third step is performed by:

forming said third polycrystalline silicon layer on the whole surface of said substrate to allow said first and third polycrystalline silicon layer to be connected to each other via said contact hole on said first polycrystalline silicon layer formed during said second step, and forming said silicide layer on said third polycrystalline silicon layer;

forming a photoresist pattern on the whole surface of said substrate, and sequentially etching said silicide layer said third polycrystalline silicon layer, said second polycrystalline silicon layer, said interlayer insulating film, and said first polycrystalline silicon layer, using said photoresist pattern as a mask, to simultaneously form a double-level gate electrode of said storage cell transistor in said cell array region and a gate electrode of the transistor in which gate electrodes of double-level are connected to each other in said peripheral circuit region; and

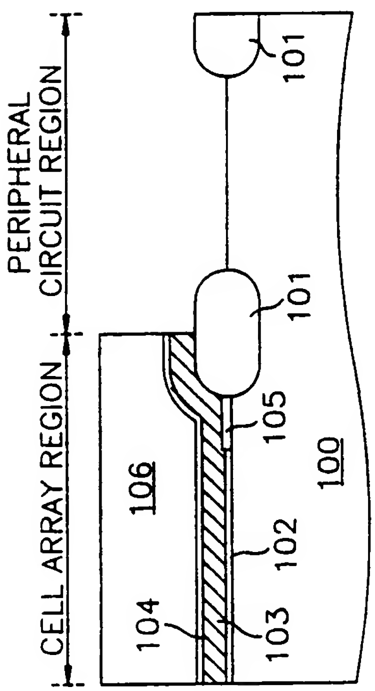
carrying out an ion-implantation onto the whole surface of said substrate, and then onto said source and drain regions of said storage cell transistor and said source and drain regions of said transistor in said peripheral circuit region, using said photoresist pattern as a mask.

14. A method for manufacturing a semiconductor memory device as claimed in claim 12, wherein said interlayer insulating film is a multi-level insulating layer obtained by sequentially stacking oxide layer, nitride layer and oxide layer.

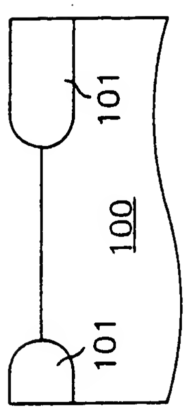
15. A method for manufacturing a semiconductor memory device as claimed in claim 12, further comprising an etching step of removing a natural oxide layer on the surface of said second polycrystalline silicon layer before forming said third polycrystalline silicon layer.

16. A method for manufacturing a semiconductor memory device as claimed in claim 12, wherein said metal layer in said peripheral circuit region contacts with said third polycrystalline silicon layer via said silicide layer around said contact hole in which said third and first polycrystalline silicon layers are connected to each other.

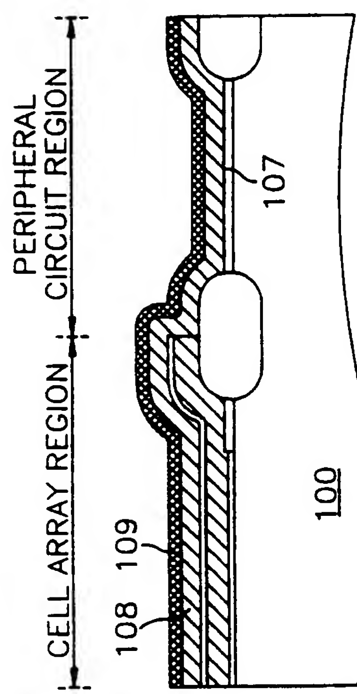
17. A method for manufacturing a semiconductor memory device as claimed in claim 12, wherein said silicide layer is formed of tungsten silicide.



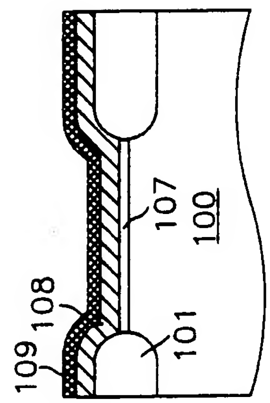
(PRIOR ART)
FIG. 1A



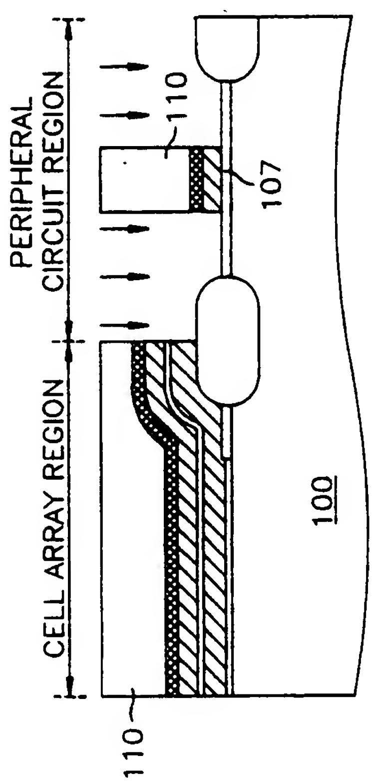
(PRIOR ART)
FIG. 1B



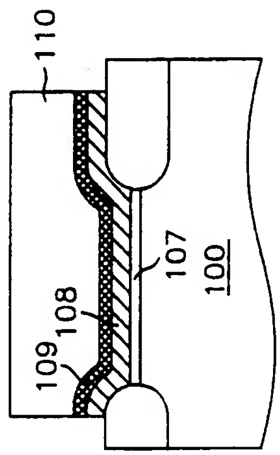
(PRIOR ART)
FIG. 1C



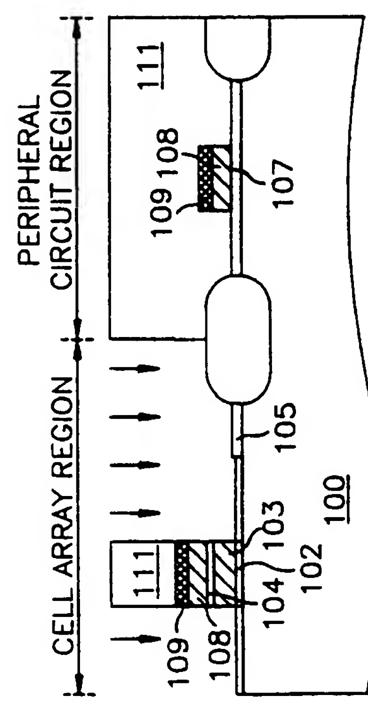
(PRIOR ART)
FIG. 1D



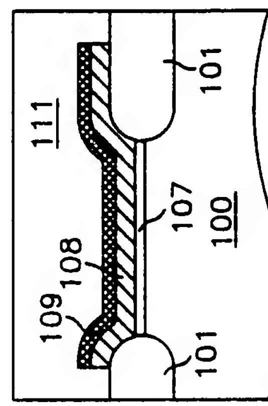
(PRIOR ART)
FIG. 1E



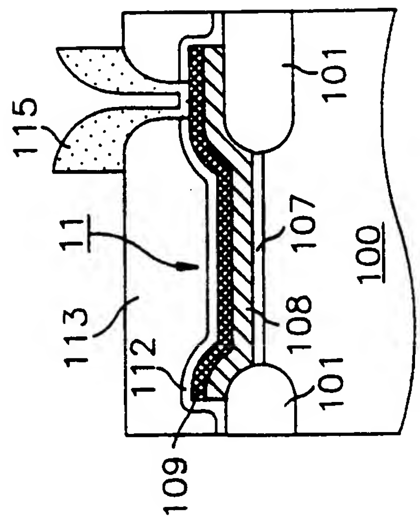
(PRIOR ART)
FIG. 1F



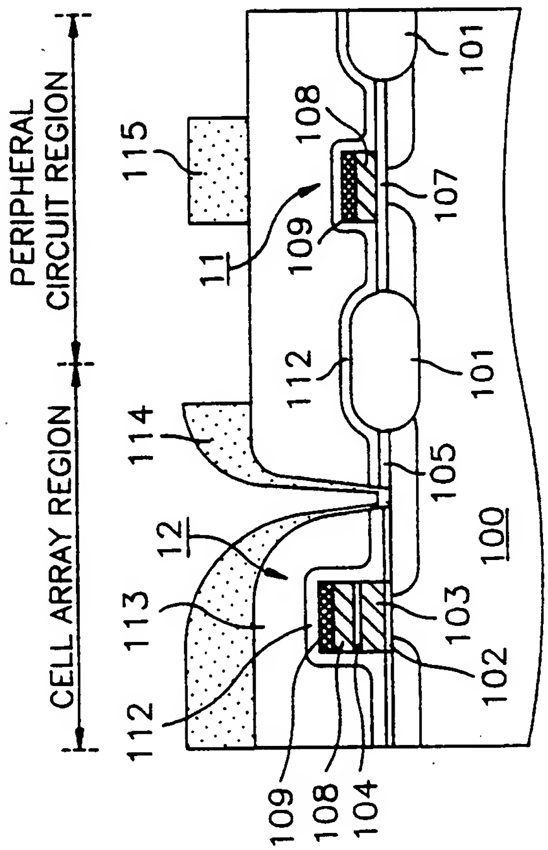
(PRIOR ART)
FIG. 1G



(PRIOR ART)
FIG. 1H



(PRIOR ART)
FIG. 1J



(PRIOR ART)
FIG. 1I

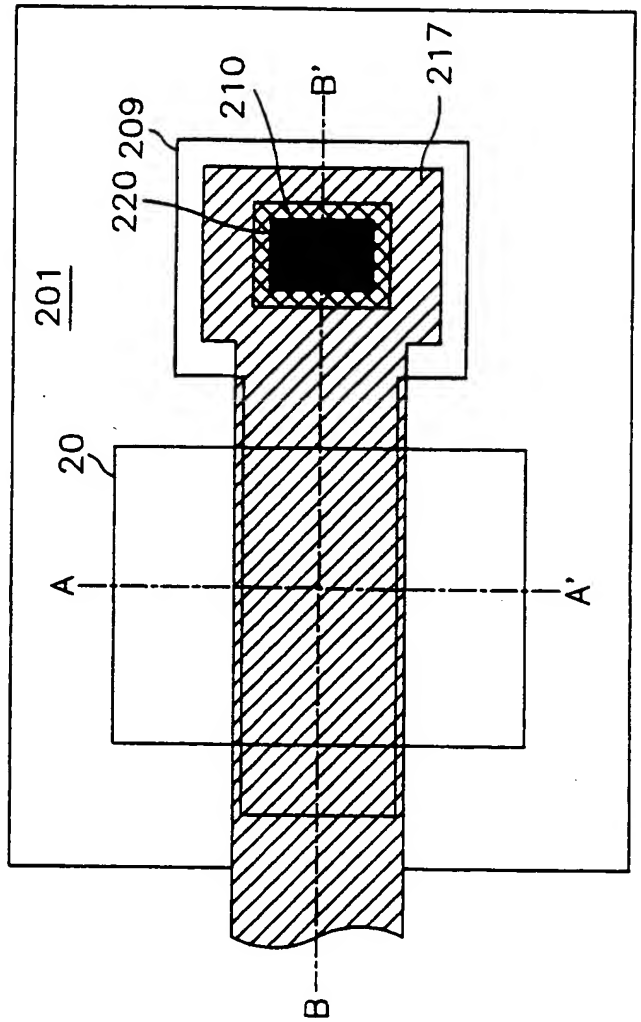


FIG. 2

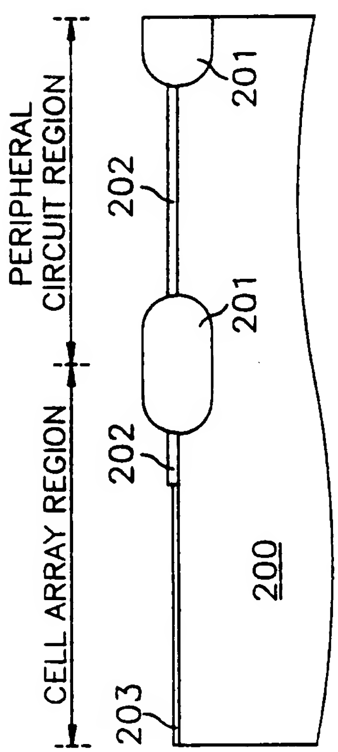


FIG. 3A

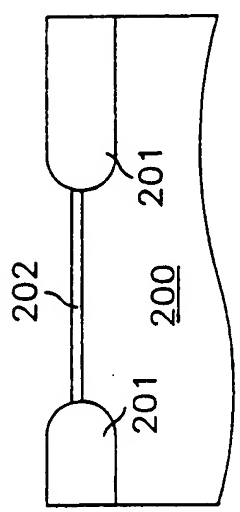


FIG. 3B

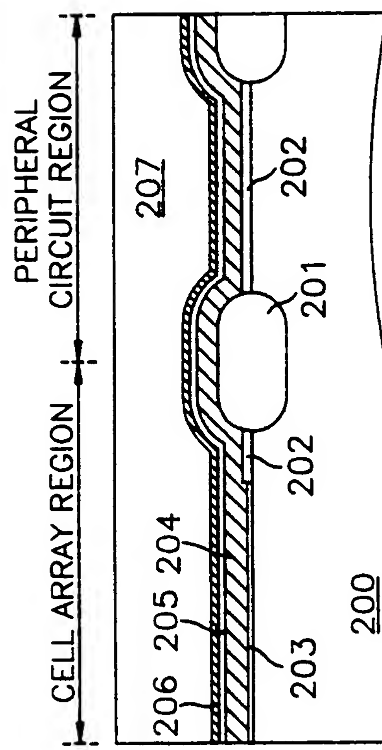


FIG. 3C

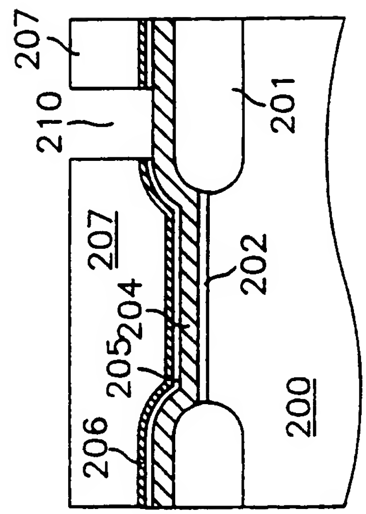


FIG. 3D

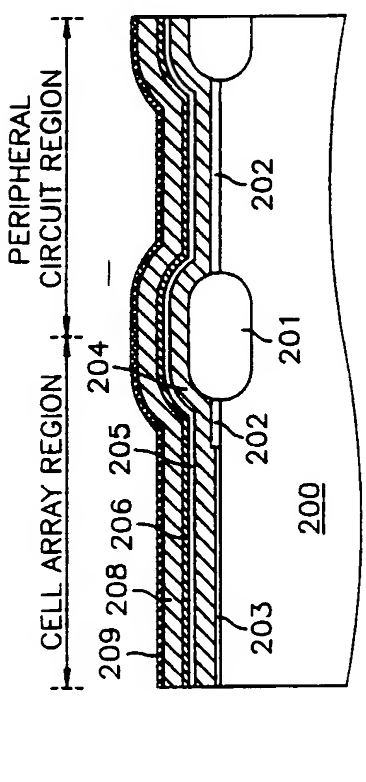


FIG. 3E

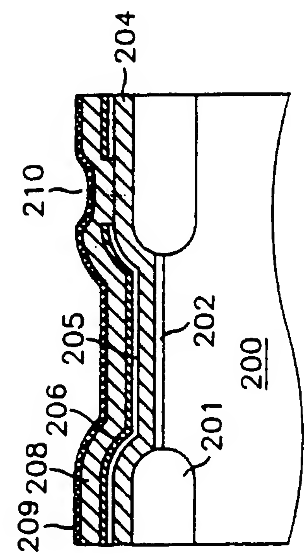


FIG. 3F

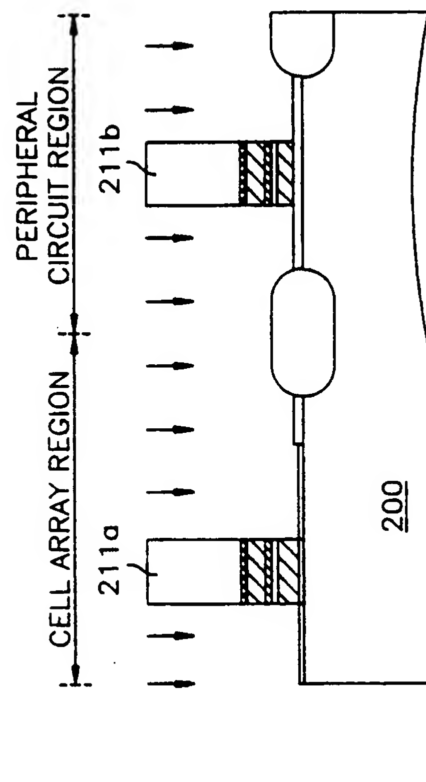


FIG. 3G

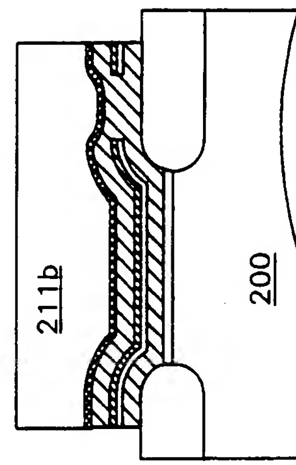
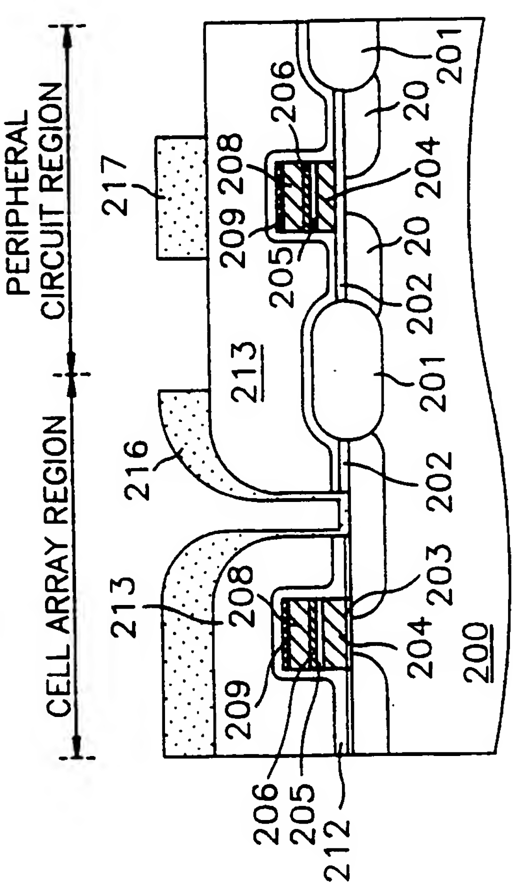


FIG. 3H


CELL ARRAY REGION
PERIPHERAL CIRCUIT REGION
213
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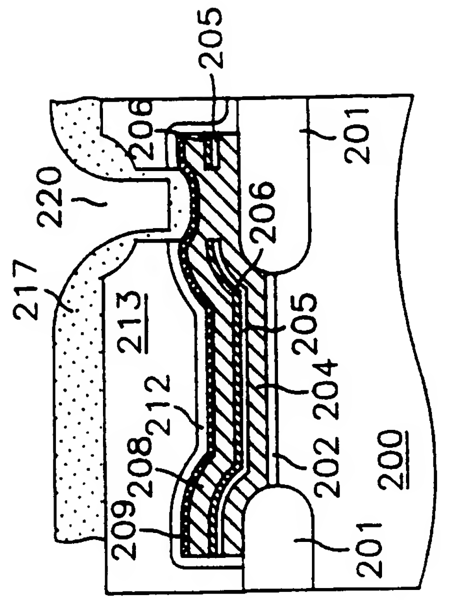
20

FIG. 3I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220
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212
208
209
204
202
200

FIG. 3J

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 93 11 2274

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X A	US-A-4 766 088 (S. KONO ET AL.) * column 4, line 37 - column 6, line 14; figures 4-11,14 *	1,2,7,8 12,16	H01L27/115 H01L21/82
X	PATENT ABSTRACTS OF JAPAN vol. 011, no. 396 (E-568)24 December 1987 & JP-A-62 156 875 (NEC) 11 July 1987 * the whole document *	1,2,7,8	
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 476 (E-1140)4 December 1991 & JP-A-32 05 870 (NEC) 9 September 1991 * the whole document *	1,7	
A	US-A-5 032 881 (G. M. SARDO ET AL.) * column 4, line 61 - column 5, line 19; figure 4 *	3,4,9, 10,12,14	
A	US-A-4 663 645 (K. KOMORI ET AL.) * column 11, line 53 - column 12, line 68; figure 13 *	5,6,11, 17	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	13 SEPTEMBER 1993	JUHL A.

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